Substrate Loss Mechanisms for Microstrip and CPW Transmission Lines on Lossy Silicon Wafers

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Abstract—**Loss mechanisms for microstrip and coplanar transmission lines on lossy silicon substrates are analyzed. It is shown that the losses are bias-dependent. This is supported both by experimental results and numerical simulations. We attribute this effect to changes in the carrier static distribution underneath the oxide. A continuous analysis of the losses is performed from accumulation to strong inversion. It demonstrates that neglecting the variations of RF losses versus DC bias conditions can lead to important inaccuracies on the extracted values of circuit and device physical parameters.**

I. Introduction

Microstrip lines (MS) and coplanar waveguides (CPW) are widely used in MMIC's as interconnects and matching networks. Designing low-loss transmission lines is a key factor to obtain high performance MMIC's in silicon technology. A good understanding for loss mechanisms of CPW and MS lines is therefore crucial. In [1] and [2], Reyes *et al.* reported that CPW losses increase if an insulating SiO_2 layer is grown between the silicon and the metal lines. They attribute this effect to the presence of free carriers at the silicon/oxide interface, which locally increases the substrate surface conductivity . In [3] Wu *et al.* experimentally showed through a quasi static C-V technique that an induced charge layer exists at zero bias underneath the oxide of their studied structure. In both studies no RF measurements of CPW were performed for other bias value than zero volt. In current applications however DC bias is usually added to the RF signal propagation along the CPW or MS line. This DC bias supply is approximately 1-3 V for CMOS circuits and typically higher than 10 V for MEMS devices [4].

In this work we investigate further on the effects of an applied DC voltage on RF losses for both CPW and MS lines. Through experimental and simulation results we show that losses increase when an accumulation or an inversion layer exists at the insulator/silicon interface. We also compare the dependence of losses vs DC bias conditions for two types of oxide qualities and show that the presence of interface traps influences this dependence. A continuous analysis of the effects of DC conditions on RF losses is actually performed for both CPW and MS lines over the entire range from accumulation to strong inversion.

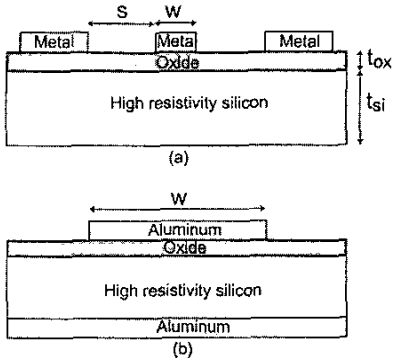

Fig. 1. CPW (a) and MS (b) structures under analysis.

TABLE I
STUDIED STRUCTURES

	Metal	Oxide	t_{ox} [nm]	t_{si} [μm]
CPW 1	Au/Ti	none	none	500
CPW 2	Au/Ti	PECVD	500	500
CPW 3	Au/Ti	Thermal	500	500
CPW 4	Alu/Ti	Thermal	500	500
MS 5	Alu	APCVD	240	500
MS 6	Alu	Thermal	300	500

II. Measurements

Four different types of CPW lines (Fig. 1a) and two types of MS lines (Fig. 1b) are measured. In all cases the substrate is a high resistivity ($> 5\ k\Omega.cm$) p-type silicon. Both CPW and MS lines are designed for a characteristic impedance of 50 Ω. The central conductor width of the CPW lines is $w = 24\ \mu m$ and the line spacing is $s = 40\ \mu m$ for a 500 μm-thick Si substrate. The strip width of the MS line is $w = 430\ \mu m$ for a 500 μm-thick Si substrate. As summarized in Table I, the metal layers used are Au/Ti, Alu/Ti and Alu with a 1 μm-thickness for each. CPW 1 is characterized by a direct contact between the lines and the silicon. In CPW 2, 3 and 4 a 500 nm-thick SiO_2 insulating layer exists on top of the silicon surface. CPW 2 and 3 only differ by the quality of their oxide layer and their $SiO_2 - Si$ interface

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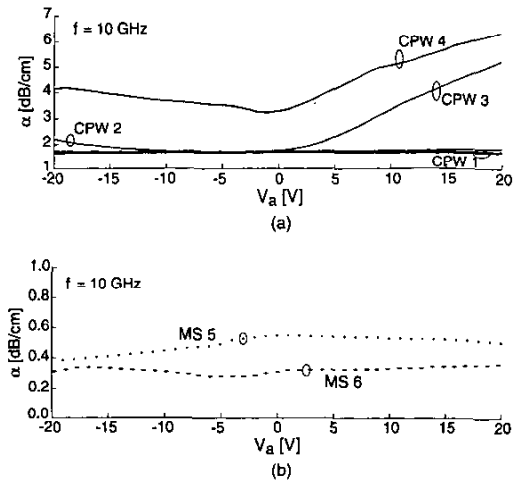

Fig. 2. Measured CPW (a) and MS (b) losses vs DC bias at 10 GHz.

in terms of oxide charge and interface trap densities. Two distinct oxide qualities are also tested on MS 5 and MS 6. For the measurements the CPW central conductor and the MS strip are successively biased from -20 V to 20 V with 1 V steps. At all polarization points the scattering parameters of the lines are measured from 40 MHz to 40 GHz with a Wiltron 37369A vector network analyzer.

Fig. 2a displays the variations of the attenuation constant at an arbitrary frequency of 10 GHz for the four CPW lines. The curves outline the same features at all measured frequencies in the 0.04-40 GHz band. In such structures, the conductor losses are estimated by IE3D simulations to be around 1.5 dB/cm at 10 GHz. From these data it appears that: (1) within the entire bias range only the losses for the thermal oxide-passivated structure are bias-dependent; (2) the attenuation constant of the thermal oxide-passivated CPW increases for both strong negative and positive DC biases and reaches a minimum for a small negative DC bias value. The curves also indicate that this increase is non-symmetrical: losses increase more rapidly for positive than for negative voltages. The measurements performed on the MS lines are presented in Fig. 2b and show that the attenuation constant only slightly varies throughout the entire bias range.

III. Interpretation

The experimental results presented in the previous section can be qualitatively and simply explained by semiconductor physics theory. The local conductivity of silicon is given by:

$$\sigma = q(\mu_n n + \mu_p p) \tag{1}$$

where μ_n, μ_p, n and p, respectively, denote the local mobility of electrons and holes, and the local concentration of electrons and holes. This equation takes on very simple forms when one carrier type is found in much higher density than the other: for $n \gg p$ and $n \ll p$ we have respectively:

$$\sigma \cong q\mu_n n \tag{2a}$$

$$\sigma \cong q\mu_p p \tag{2b}$$

These expressions indicate that the silicon conductivity is an increasing function of free carrier densities in the substrate. By modifying carrier concentrations at the silicon surface we can change the substrate surface conductivity, and hence losses along the analyzed lines. These concentrations strongly depend on the surface electrostatic potential (ϕ_S). When an oxide layer exists between the lines and the silicon substrate, ϕ_S is linked to the applied voltage on the metallic line (V_a) through the following equation:

$$V_a = \phi_S + \phi_{MN} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_s(\phi_S)}{C_{ox}} - \frac{Q_{it}(\phi_S)}{C_{ox}} \tag{3}$$

In (3), ϕ_{MN}, Q_{ox}, C_{ox}, Q_s and Q_{it}, respectively, denote the contact potential between the metal and the bulk $[V]$, the fixed oxide charge density $[Cb/cm^2]$, the oxide capacitance $[F/cm^2]$, the equivalent surface charge density of the bulk $[Cb/cm^2]$ and the interface trapped charge density $[Cb/cm^2]$. Q_{it} is also a function of ϕ_S [5].

According to (3) four major factors were identified to influence the value of ϕ_S: (1) the presence of an oxide layer between the lines and the substrate; (2) the DC bias of the line, (3) the densities of oxide charges and (4) interface traps at the SiO_2/Si interface.

For a direct metal/silicon contact, interface trap density is very high and the value of ϕ_S is pinned to a level determined by the trap properties [6]. As a result, free carrier densities at the silicon surface are maintained to a very low value regardless of the applied DC bias. As shown in Fig. 2a, CPW 1 losses are relatively bias-independent and are the lowest in all the measured bias range. These measurements are in agreement with the experimental results presented in [1] and [7] that reported at zero bias the lowest losses for CPW lines directly deposited on high resistivity silicon substrate.

When an oxide layer exists between the lines and the silicon (as in CPW 2, 3 and 4) the static charge distribution in the system is largely modified and can be strongly influenced by the applied bias. For a p-type semiconductor, the region under the line successively switches from accumulation to depletion and then strong inversion when the applied DC bias is raised from -20 V to +20 V. For this reason, CPW 3 and 4 losses are high for negative and positive voltages and reach a minimum value when the substrate surface under the central line is depleted from free carriers. This is shown by both experimental (Fig. 2a) and simulation curves obtained with the Atlas software of Silvaco (Fig. 3a - solid line). The simulation curves display the variations in % of

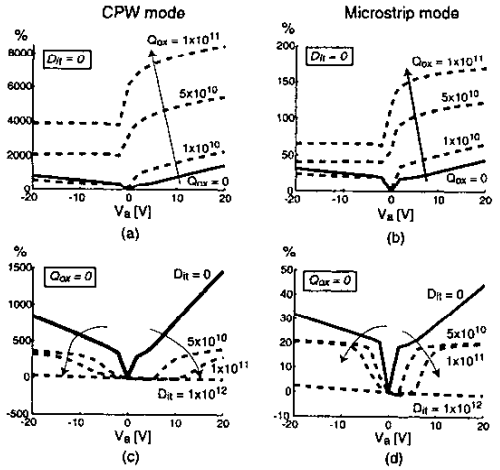

Fig. 3. Simulation results: relative variations of the shunt conductance for both CPW (a and c) and MS (b and d) with respect to V_a and for different values of D_{it} and Q_{ox}.

the distributed equivalent shunt conductance (G) of a TEM-mode transmission line. For all curves the reference value of G is taken at $V_a = Q_{ox} = D_{it} = 0$. One can also see from Fig. 2 that the losses are higher for the CPW 4 line due to the higher resistivity of aluminum compared to that of gold.

Losses are also increased when the oxide layer contains fixed positive charges that attract electrons towards the interface. In the case of a p-type silicon substrate a thin inversion layer is formed at the SiO_2/Si interface covering the entire silicon surface. Simulations of CPW 3 with increasing values of Q_{ox} show the influence of oxide charges on the shunt conductance of the line (Fig. 3a).

Interface traps at the SiO_2/Si interface capture free carriers from the substrate, which leads to a decrease in free carrier concentration underneath the oxide. In mathematical terms the presence of interface traps flattens the ϕ_S vs V_a curve [5], and thus reduces the influence of V_a on surface free carrier densities. The influence of D_{it} was simulated on CPW 3. The simulation results are shown in Fig. 3b: traps have the effect to increase the bias range for which the silicon region under the line is in depletion state. For large values of D_{it} this region extends over the entire studied DC bias range. In that case the influence of V_a is almost suppressed and the shunt conductance is kept to its lowest value. The much larger values of D_{it} yielded by PECVD processes could provide an explanation for the observed lower (and quasi bias-independent) losses of CPW 2 compared to losses of CPW 3 and 4 (Fig. 2). These results are in agreement with the ones obtained in [7] where Gamble *et al.* reported at zero bias that losses on a polysilicon-stabilized HRS substrates with high interface trap density are lower than on oxide-passivated substrates.

Losses on MS also appear to be influenced by the value of the applied bias (Fig. 2b). MS 6 measurements follow the trend outlined by the simulation curve of Fig. 3a (thick line): losses are higher when the substrate underneath the oxide is in state of accumulation or depletion. The MS 5 measurement curve in Fig. 2 however behaves according to an opposite fashion: α reaches a peak value around $V_a = 0\ V$. This structure is actually submitted to the influence of a high trap density at its Si/SiO_2 interface. Fig. 3d shows that the effect of interface traps on the shunt conductance of the MS line is similar to its influence on the CPW structure: increasing values of D_{it} widen the depletion bias range. A value of $D_{it} = 5.10^{11}\ \#/cm^2/eV$ is enough to almost completely suppress the influence of V_a. The fact that the MS 6 curve exhibits an opposite behaviour than that predicted by the curves in Fig. 3d is probably the result of a complex interaction between interfering elements: a high value of Q_{ox}, a high value of D_{it} as well as D_{it} variations with respect to V_a. It has indeed been shown in [8] that high electric fields could lead to reversible or irreversible trap formation in MOS structures.

It should nevertheless be noted here that the relative variations of α are much less important for the MS than for the CPW structures despite the thinner oxide of the MS structure: they remain lower than 35% for both MS 5 and MS 6 throughout the entire bias range at 10 GHz while CPW 3 measurements outline loss variations of the order of 200% at 10 GHz. These low variations are also observed in the simulation curve displayed in Fig. 3c (thick line). As a matter of fact, a major difference prevails between both structures: some of the electric field lines are parallel to the induced charge layer in CPW lines while they are all perpendicular to the charge layer in the MS structure. Since this layer only extends over a few microns inside the substrate, the conductive movement of free carriers is therefore much more limited in MS than in CPW structures. Consequently the effects of V_a is much less critical in MS than in CPW structures. This is also outlined by the influence of oxide charges on the structure: increasing Q_{ox} by the same factors leads to almost double the shunt conductance of the CPW structure while it barely yields a 40% increase for the shunt conductance of the MS line (Fig. 3a and b).

IV. Discussion

The observed loss variations with respect to the applied DC bias in the case of CPW 3 or 4 should be taken into account in the measurements of devices requiring a calibration procedure. The calibration step is usually necessary to evaluate the electrical properties of access lines. The device under test as well as the calibration kit elements should be measured under the same DC conditions because the electrical properties of the access lines vary according to their DC conditions. The error introduced by neglecting this effect can become critical in some cases. For example, the

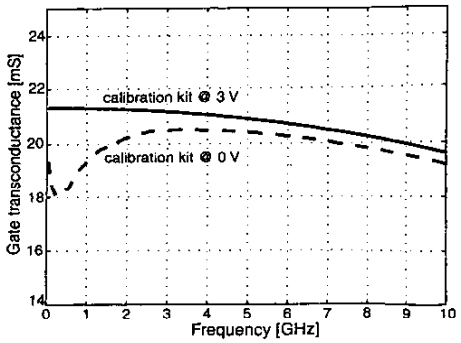

Fig. 4. Intrinsic gate transcondutance of a MOSFET extracted from RF S-measurements: correct (solid line) and erroneous (dashed line) curves.

intrinsinc gate transconductance (g_m) of a MOSFET is extracted from the real part of the Y_{21} parameter. Fig. 4 shows the g_m curves obtained when the MOSFET is measured at both V_g and $V_d = 3\ V$. The correct (solid line) curve is obtained if the S-parameters of the transistor are de-embedded when the calibration kit is measured under 3 V. An erroneous curve is obtained when the calibration kit is measured at 0 V. At a frequency of around 250 MHz the committed error is about 20%. This can have negative consequences on the overall electrical characterization of the transistor and subsequently in the design of analog circuits. The error introduced is of course directly dependent on the access line length. In our case, 45 μm-long CPW were used to access the transistor ports.

The experimental results presented above clearly indicate that a drastic reduction of substrate losses in CPW structures can be obtained when the substrate surface is depleted from majority carriers. Several ideas have been proposed in the literature to reduce the induction of charges at the silicon surface. In [3] Wu *et al.* suggests to etch the oxide layer between the signal and ground tracks in order to avoid the negative effect of oxide charges in these areas. The same authors also proposed to introduce a stabilizing layer of polycristalline silicon between the oxide and the substrate as the polycristalline/substrate interface is characterized by a high interface trap density [7]. SiO_2 was then introduced between the lines and the polycristalline Si to prevent DC current leakage. The main disadvantage of these two successful solutions is the additional step required in the fabrication process. Still in [7], the best improvement was obtained with a non-passivated substrate. The problem in that case is the existence of a DC leakage current flowing from the signal to the ground tracks.

The curves in Fig. 2 suggest two other solutions to reduce the losses. For a thermal oxide-passivated layer, a practical solution is to design the passivation layer in such a way as to place the minimum loss point of the curve at the middle of the application bias range. This requires however a good knowledge of the technological process parameters. A more simple solution is to use a CVD instead of thermal oxide to passivate the substrate. As shown in Fig. 2, this type of oxide contains enough interface traps to absorb free carriers from the silicon surface and almost suppress the bias dependence of the losses. This solution does not require any additional step in the fabrication process. It also presents the advantage of an oxide deposition at low temperature.

V. Conclusion

The study of the losses in both CPW and MS structures indicate that CPW losses are much more influenced by the presence of free carriers under the line metal. This is because part of the electric field lines are parallel to the induced charge layer in the CPW structures while they are all perpendicular in the MS structure. As a consequence, CPW losses can vary significantly with the applied DC bias (20% increase from 0 to 3 V in one of our studied structures). Neglecting this effect can have negative consequences in RF-measurements because it introduces errors in calibration procedures. However, these variations are drastically reduced when the SiO_2/Si interface is characterized by a high interface trap density. As shown in this work, LPCVD-deposited oxide appears in this context as a very suitable candidate to passivate the silicon surface in high-resistivity substrate MMIC's. It also presents the advantage of being a low cost, low temperature process.

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